PATENT
Attorney Docket No. 915-001.090

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

Ari PEKKARINEN et al	:	Confirmation No. **6761**
Serial No: **10/582,833**	:	Examiner: **Feifei Yeung Lopez**
Filed: **June 14, 2006**	:	Group Art Unit: **2826**

For: **METHOD AND ARRANGEMENT FOR SHIELDING AN ELEMENT AGAINST ELECTRASTATIC INTERFERENCE**

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REPLY BRIEF

Sir:

This Reply Brief is in response to the Examiner's Answer of August 26, 2010, and in furtherance of the Appeal Brief filed July 2, 2010 appealing the rejection of claims 1-20.

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Briefs-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Cathy Sturmer — 10.19.10
Cathy Sturmer — Date

REMARKS

In response to the Examiner's Answer of August 26, 2010, appellant respectfully submits that the rejections to the claims are incorrect for at least the arguments presented in the Appeal Brief filed July 2, 2010. In addition, appellant responds to the points raised in the Examiner's Answer as follows.

With regard to Hong the Office points to layer (105), in Figure 4 to be the claimed electroconductive metal element of claim 1. However, appellant respectfully disagrees. Even if the layer (105) of Hong is constantly connected to ground the layer (105) does not shield the semiconductor element (102) against electrostatic pulses as disclosed in claim 1. Hong does not teach that the layer (105) alone has the purpose to shield the semiconductor element (102) against electrostatic pulses. Instead, Hong teaches that there is always needed a non-ohmic material element to cooperate with the layer (105) in order to shield the semiconductor element (102) against electrostatic pulses. See Hong column 4, lines 1-16, 18-32 and 37-57; Figure 3 & 4. The discharging member of Hong is also described to act as conductorinsulator in order to protect the chip from ESD impacts. See Hong column 2, lines 10-13 and 23-29. Therefore, Hong does not disclose an integrated electroconductive metal element comprising at least one outlet, wherein the at least one outlet is configured to constantly connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses, as recited in claim 1. In addition, Hong does not disclose or suggest that at least one outlet of the electroconductive metal element is constantly connected to ground, as recited in claim 1, because of the varistortype (conductor-insulator) characteristics of the discharging element of Hong.

With regard to Sherwood the Office points to layer (75), in Figure 3 to be the claimed electroconductive metal element of claim 1. However, appellant respectfully disagrees. Sherwood teaches that cooperation of Mylar faceplate (42) and conductive surface (75) is required to protect the microprocessor (103) from ESD. See Sherwood column 4, lines 57-65. This means that in Sherwood there is needed a combination of dielectric Mylar faceplate (42, 71) and conductive surface (75) in order to shield the semiconductor element (103) against electrostatic pulses as disclosed in claim 1. Sherwood does not teach that the conductive surface (75) alone, even if constantly connected to ground, has the purpose to shield the semiconductor element (103) against electrostatic pulses. The conductive surface (75) alone does not

correspond the electroconductive metal element disclosed in claim 1. Therefore, Sherwood does not disclose an integrated electroconductive metal element comprising at least one outlet, wherein the at least one outlet is configured to constantly connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses, as recited in claim 1. Furthermore, Sherwood also fails to disclose or suggest that at least one outlet of the electroconductive metal element is constantly connected to ground, as recited in claim 1, because of the conductor-dielectric (varistor-type) characteristics of the discharging element of Sherwood.

With regard to Wu the examiner points layer 24 (guard ring), in Figure 1 to be the claimed electroconductive metal element of claim 1. Appellant respectfully disagrees. Wu teaches that conductive guard ring (24) is coupled to the row and column lines (12, 14) by protection circuit elements (26). See Wu column 2, lines 28-32. Wu teaches that the protection circuit elements (26) have a substantial resistance in order to form the ESD protection structure. See Wu column 2, lines 52-57. Furthermore, Wu states that the protective circuit element couples the guard ring to the contact pad so that a transient signal applied to the contact pad is discharged to the guard ring. See Wu column 3, lines 51-54. Therefore, in Wu there is needed cooperation of the guard ring and the resistive protection circuit element in order to shield the semiconductor element (20) against electrostatic pulses. However, Wu does not teach that the guard ring (layer 24) alone, even if constantly connected to ground, has the purpose to shield the semiconductor element (20) against electrostatic pulses. The layer (24) alone does not correspond the electroconductive metal element disclosed in claim 1. Therefore, Wu does not disclose an integrated electroconductive metal element comprising at least one outlet, wherein the at least one outlet is configured to constantly connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses, as recited in claim 1. In addition, Wu also fails to disclose or suggest that at least one outlet of the electroconductive metal element is constantly connected to ground, as recited in claim 1, because of the resistor characteristics incorporated in the protection circuit element (26) of Wu used to form the ESD protection structure with the guard ring (24). Furthermore, in Figure 9 of Wu, a combination of guard ring (130) and CCFET (50) have similar effect as discussed above.

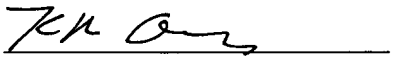
In addition to the distinctions between the cited references and claim 1 discussed above, the cited references also do not disclose or suggest the limitation of encased by a cover element having an integrated electroconductive metal element, as recited in claim 1. Sherwood does not teach that the faceplate (42) and conductive surface (75) would be integrated in the cover (21, 22). Wu does not teach that the guard ring (24) and the protection circuit element (26) would be integrated in the cover of the display panel.

Conclusion

It is respectfully submitted that the present invention as claimed is readily distinguishable over the cited references. Appellants' invention is not disclosed in the applied cited references and there is no fair basis for alleging that appellants' invention is obvious in regard to such references. In view of the above, it is respectfully submitted that the rejections of claims 1-20 are in error and must be reversed. Such reversal is earnestly solicited. The undersigned hereby authorizes the Commissioner to charge Deposit Account No. 23-0442 for any fee deficiency required to submit this response.

Respectfully submitted,

Date: 19 October 2010



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